Pixel Electronics Status at LBL

Overview of Activities for Demonstrator Chip (FE-B):

- Progress on Front-end design
- Progress on Readout Architecture
- Progress on System Integration

Progress on Demonstrator FE-B Chip Design

Front-end Design:

- Have submitted three generations of prototypes for next-generation front-end design, including 3 MOSIS and one Honeywell submission.

  → First generation submitted in Sept. 96 (HP only) tested initial ideas for preamplifiers and feedback, and dual-threshold discriminator design. Many lessons learned... Discarded low-pass filter coupling circuit, improved LBL feedback scheme, evolved from two independent discriminator scheme.

  → Second generation submitted in Feb. 97 (HP and Honeywell) included improved frame, new dual threshold design using single differential amplifier plus single dual-threshold discriminator. Also used AC-coupling for CPPM feedback design. Now under test in lab.

  → Third generation submitted in May 97 (HP only) including realistic layouts, improved LBL feedback scheme, all DC-coupled for comparison to previous case, and implementing new tuning concept.

- Now have essentially final design, and most recent submission will allow detailed characterization and final validation before making wafer-scale submission

Readout Architecture:

- Have submitted new design in May 97 (HP only). It is a complete prototype of the basic building block: a column pair and its End-of-Column logic with concurrent input and output support.
- Remaining design issues within column-pair will be addressed, prototype chip will be evaluated for possible optimizations or improvements.

- Remaining circuit blocks required to connect together column pairs are specified, and will be designed and simulated (no prototype foreseen at this time, but possibility of ”small array” submission in July ?).

System Integration:

- Design started on additional functional blocks, but schedule does not permit prototyping (they are simple, but...)

  → Digital bias control (“current-mode DACs”): under design

  → Command Decoder and associated registers: design exists, Verilog simulated, but not yet finalized for layout, pending final “freezing” of specifications

- Presently working on complete Cadence block diagram (see later talk for definitions of all blocks)
- Major issue will be integrating and verifying the complete chip: expect it to exceed the 1M transistor mark - a first for HEP ?

Test Results from Second Generation Prototype

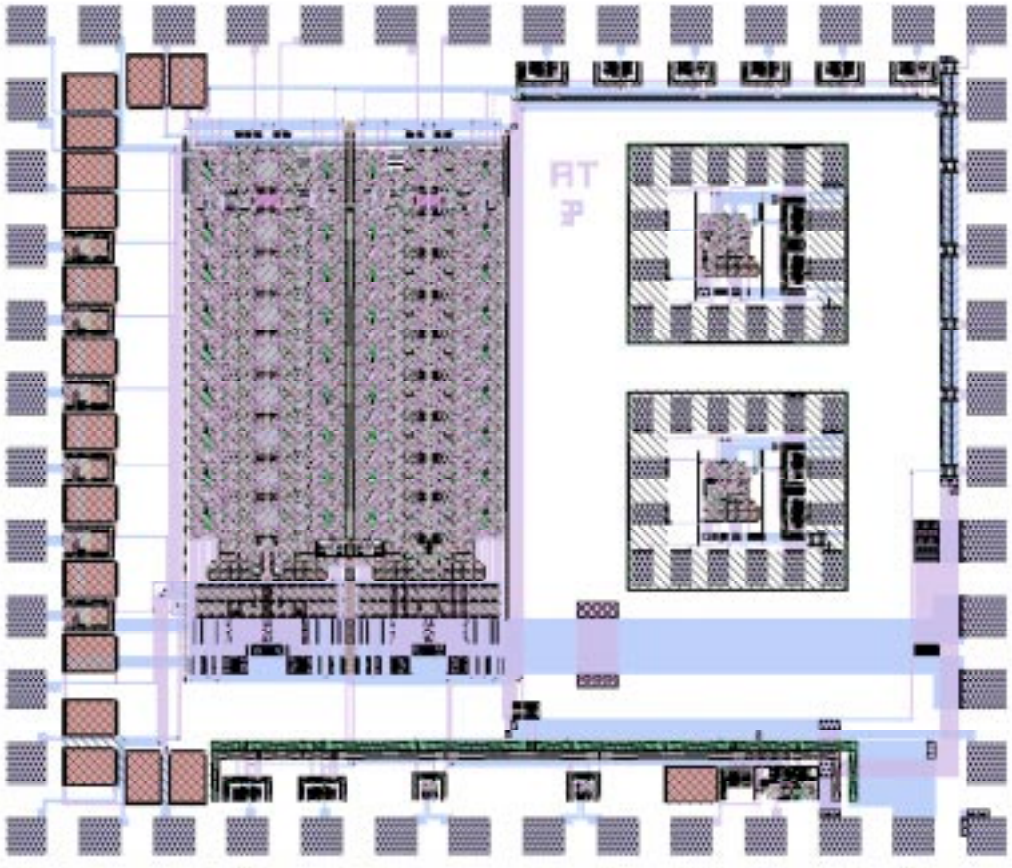
First results for CPPM feedback scheme:

- Gain is ≈ 250 mV/fC
- Risetime is ≈ 20 ns for a power of ≈ 35 μW
- Feedback currents now in few nA range (poor current mirroring in first chip ?), still about a factor of 2 off from simulation.
- Noise ≈ 60e without capacitive loading
- New discriminator without latching output provides good threshold separation between Low and High (e.g., 2Ke and 4Ke are easily achieved).
- Timewalk of 18 ns measured for 2Ke/1Ke thresholds, and 12 ns for 4Ke/2Ke thresholds (worst case timewalk from Low threshold discriminator when coincidence with High threshold discriminator is required).
- Stable with large leakage currents, but significant threshold shifts observed even with AC coupling.
- Threshold variations are small (but so is the column...)
- Many more measurements to make, but looks very likely that we will use CPPM feedback with direct active cascode, AC-coupled differential amplifier, and dual threshold discriminator for the basic front-end cell in FE-B chip.

Prototype of new LBL Pixel Front-end Design

May 7 submission of next-generation front-end designs:

- Includes 2 column pairs (18 pixels per column) with real geometry, prototype pixel control logic (Select, Mask, Calibrate, and Tune circuits), and test options.
- Contains realistic biassing and vertical power bussing. Pixel size ≈ 130-140μ



New Front-end Test Chip

Major new circuitry:

- Improved LBL feedback scheme based on improved modeling of long transistors
- Addition of new tuning scheme, based on switchable current source and current sink which adjust the reference voltage input of the differential amplifier.

  → Logic defined so that when strobed a few hundred ns after injecting charge, “below threshold” state pulses on the current sink (lowers threshold), and “above threshold” state pulses on current source (raises threshold).

  → Tuning is performed using High threshold discriminator, but moving the differential amplifier reference affects both Low and High thresholds identically.

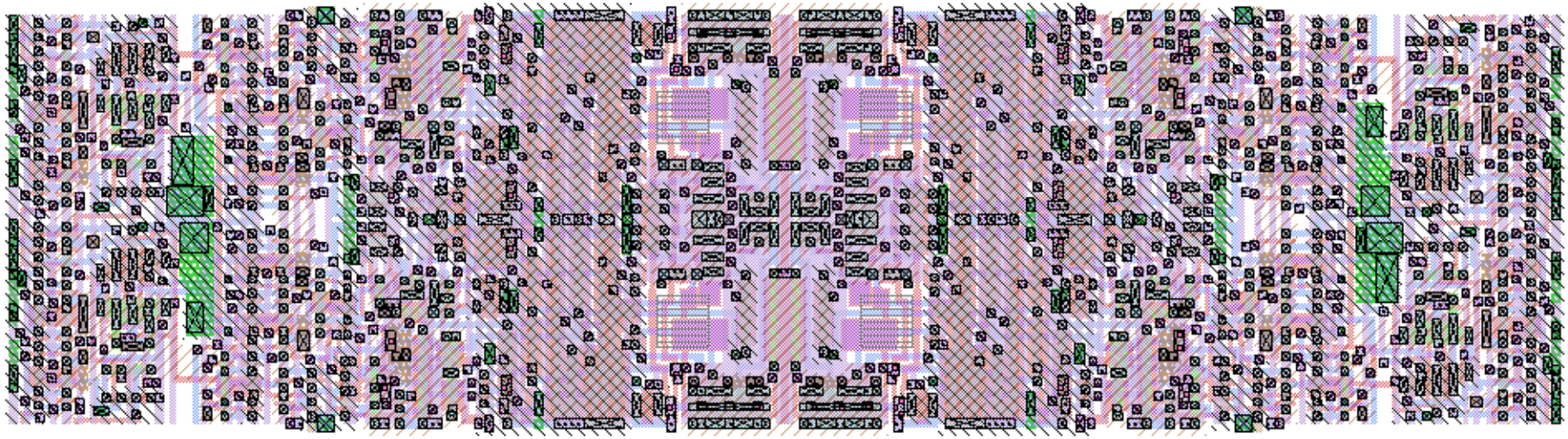
  → External signals required are simple: delayed calibration strobe whose width determines the duration of the current pulse, and correction current to determine magnitude of current pulse.

  → Circuit would nominally be operated in perhaps one pixel per column (all columns in parallel) and “stepped” through the array. One LHC abort gap could allow injection of perhaps 3-5 correction pulses. Total sweep time for array would then be 100μs x 160 = 16 ms.
- Two column-pairs implemented, one using LBL feedback scheme and one using CPPM feedback scheme, with correct geometry and input pads. Also includes correct vertical power bussing for complete 160 pixel column assuming goal of 10 mV maximum static voltage drop
- Top pixels in each column allow switching in inter-pixel coupling (≈ 50 fF) and leakage current sources (not possible in full column due to realistic geometry).

- Preamp is directly coupled to the differential amp in this version, for comparison with previous AC-coupled versions.
- The output of the dual-threshold discriminator is now non-latching (previous latch injected current and altered thresholds, and was not required).

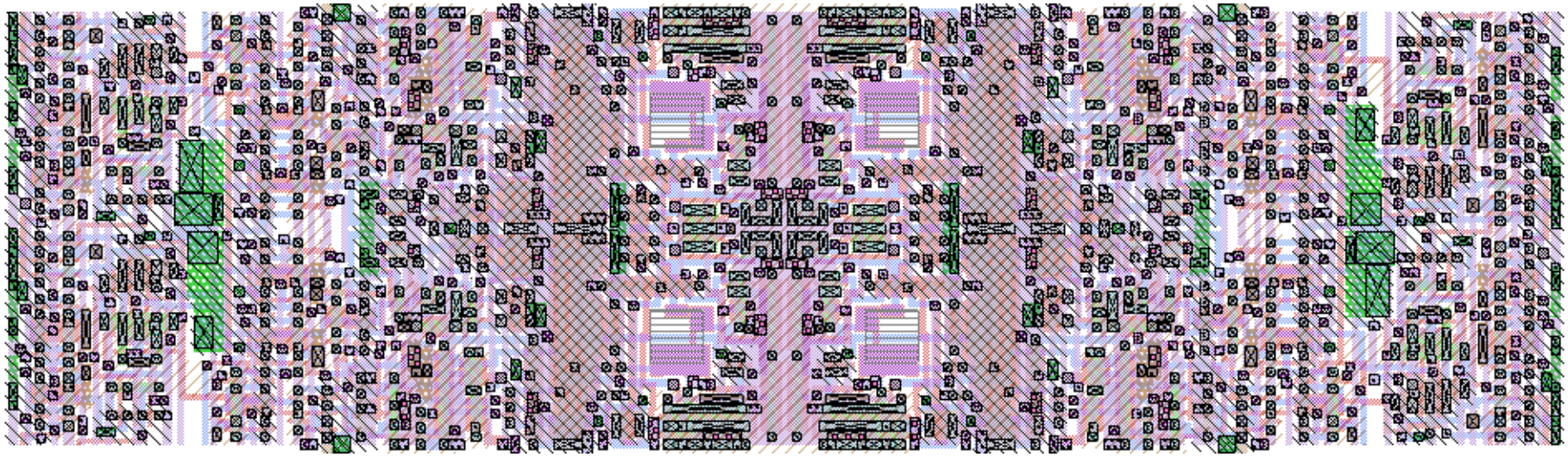
LBL Feedback Scheme

Layout of basic 4-pixel unit, size is 140μ, excluding "framing" circuitry specific to present test chip:



CPPM Feedback Scheme

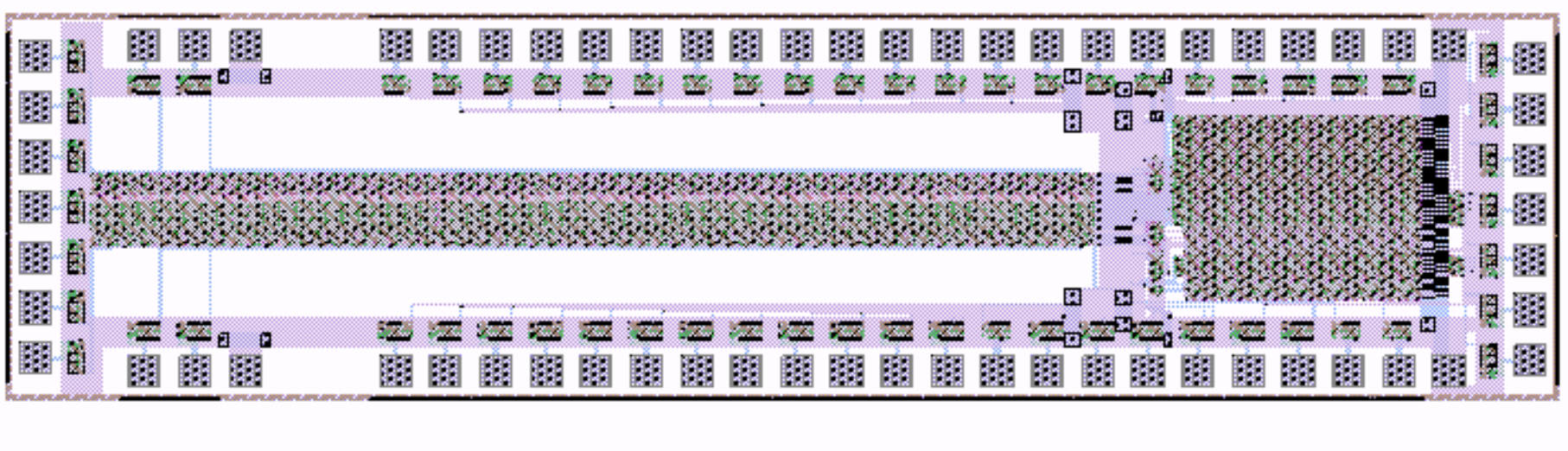
Layout of basic 4-pixel unit, size is 130μ, excluding "framing" circuitry specific to present test chip:



Prototype of new LBL Digital Architecture

May 7 submission of column-pair prototype for new architecture:

- Transmits 7-bit Grey-code timestamp to each pixel, where leading/trailing edge timing is latched
- Data is asynchronously drained from pixels to periphery as soon as it is ready
- End-of-Column logic block contains 20 buffers, capable of storing hits from up to 16 different events. Trigger accept/reject operations all performed in EOC.
- Present size: pixel back-end is 120μ, and EOC buffer block is ≈ 600μ by ≈ 1 mm



Column-Pair Interfaces

Pinout of Test Chip reflects interface to column pair:

- Left and right pixels have independent hit logic and sparse scan circuitry (ripple-through priority signal propogates down column, handshakes propagate back)
- Two-phase non-overlapping clock is used to operate delay circuitry (3 clock edges) and arbitration circuitry at bottom of column, merging two data streams into single EOC buffer block.

Chip inputs are:

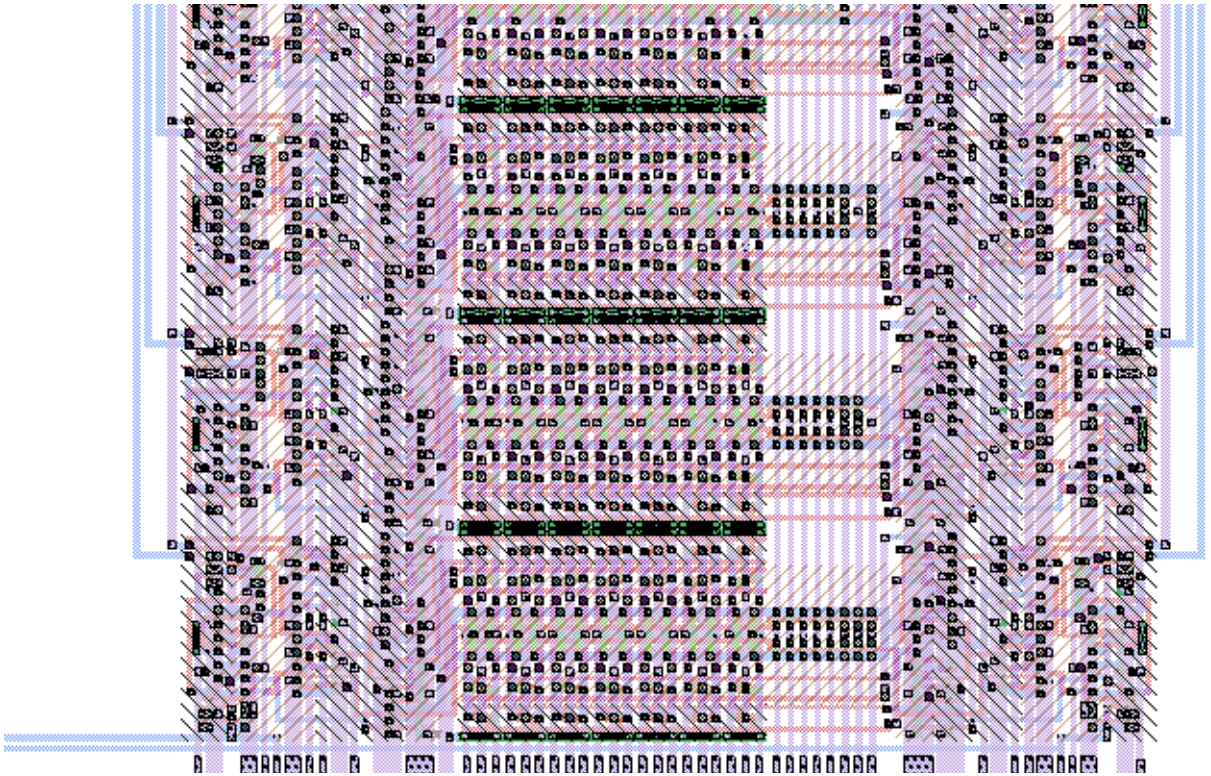
- Reset for global initialization
- Two-phase transfer clock $\phi 1$, $\phi 2$
- TSI (pixel timestamp), TSO (trigger timestamp), TAI (input trigger number), TAO (readout trigger number)
- Accept and Reject trigger control signals
- Nxt and ROCk signals for readout control

Chip outputs are:

- TEO (trailing edge output) and RO(ROM address output)
- Priority_Out handshake for readout control

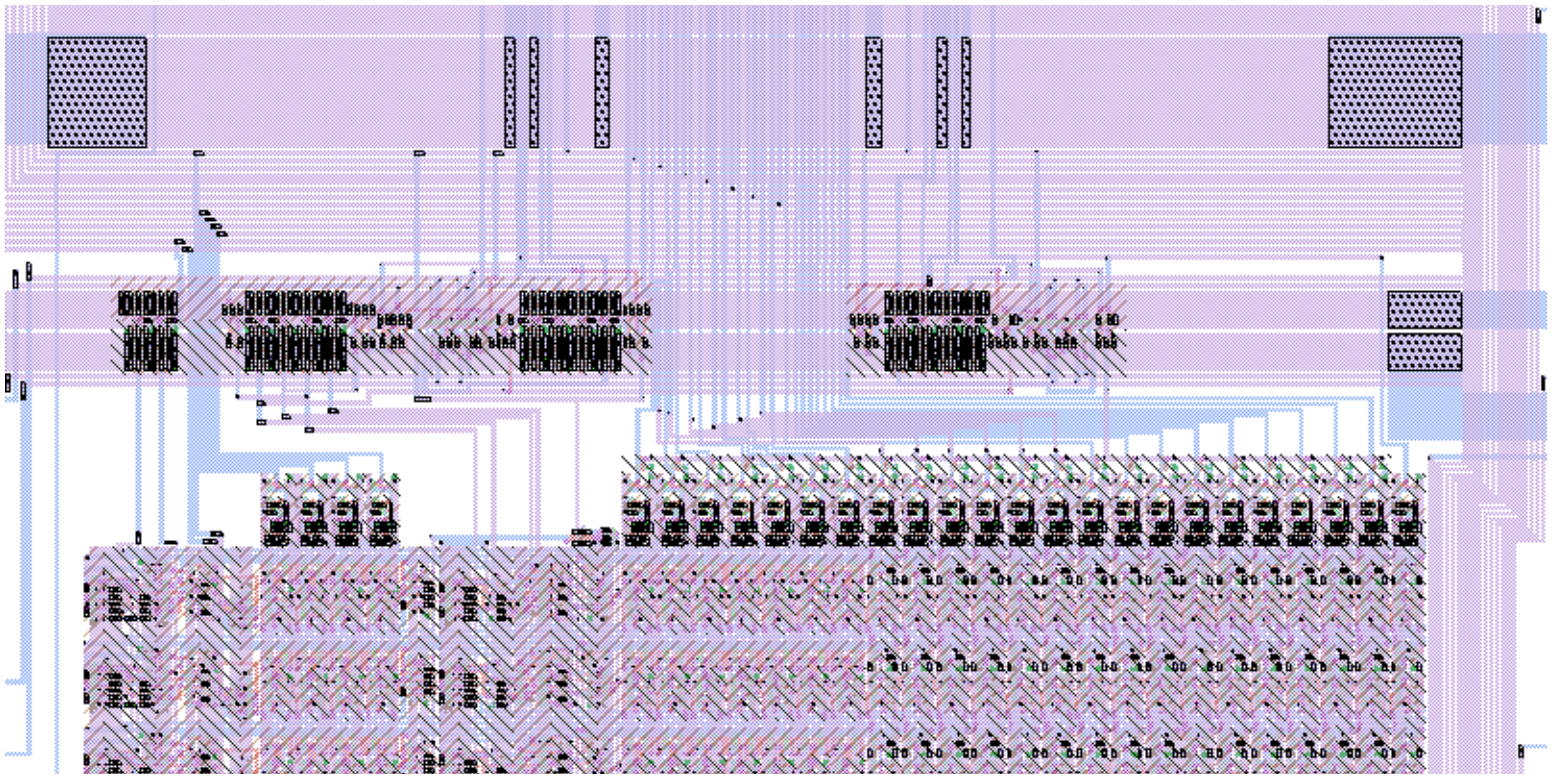
Pixel Back-end Design

Zoom view of column pair, showing hit logic for two sides, sparse scan logic for two sides, latch pair for two sides, and ROM for addresses of pixels, and common readout bus:



End of Column Buffer Design

Bottom of column circuitry followed by EOC buffer block. Single buffer spans block. Right side has storage for 7-bit TE and 9-bit Address, then 7-bit LE CAM and sparse scan circuitry for write operations. Left side has 4-bit Trigger Number CAM and sparse scan circuitry for read operations:



Next Steps

Front-end:

- Complete control logic implementation assuming new tuning will be used
- Scale up to full 2D array and make all interconnects

Readout Architecture:

- Complete optimization of column-pair for 160 pixel length (less than 1 week)
- Design additional peripheral logic blocks (clock generators and readout controller)
- Implement in complete 2D array

System Design:

- Complete design and simulation of command decoder and do layout
- Design robust clock generators for CCK distribution
- Design current-mode DACs
- Design data serializer circuitry

Do complete verification and submit (perhaps submit one last intermediate test chip in July ?)